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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/542,473	04/04/2000	Takayuki Ikeda	0756-2138	6069

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/542,473	IKEDA ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-10,16-33 and 35-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-10,16-33 and 35-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on April 26, 2004 has been entered; no new claims have been added.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 3-10,16-33 and 35-42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitation "wherein a first portion of said source wiring overlapped with said gate electrode has smaller line width than a second portion of said source wiring not overlapped with said gate electrode" recited in claims in independent claims 3, 4, 16, 18 and 35 is not disclosed in the specification to enable one skilled in the art to make and/or use the invention -- fig. 11 shows a first portion of source wiring with a smaller line width overlapping gate line 21 while a second portion of source wiring with a larger line width not overlapping gate line 21. Without this information it would take undue experimentation to make and use the claimed invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-10 and 21-25, as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto US Patent No. 5,323,042 in view of Ikeda (JP 7-326767), Otani (JP 10-56184) and Okabe (JP 63-222443).

Matsumoto discloses in fig. 1 a display device comprising a pixel portion 12 and a driver portion 13 on a substrate 11, said pixel portion comprising a semiconductor film comprising a channel forming region 21a, a plurality of impurity regions 21b, a source region 21c, and a drain region 21c; and a gate electrode 25 overlapping/partially overlapping with the channel forming region and some of the plurality of impurity regions, with a gate insulating film 24 interposed therebetween; and a source wiring 31/32 electrically connected with one of source region and said drain region, wherein a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness (as in claim 4), but omits a gate electrode overlapping plurality of channel regions/some of the plurality of impurity regions, a first portion of a source wiring with a smaller line width overlapping a gate electrode and a thicker gate film in a pixel portion than one in a driver circuit portion.

Ikeda discloses (see abstract and figs. 1-5) a display device comprising a semiconductor film having a plurality of channel regions 21 and a plurality of impurity regions 31A-C having the same conductivity type as a source 23 and drain 25 regions (as in claim 23) wherein some of

the plurality of impurity regions are located between the plurality of the channel forming regions in the semiconductor film and contain a low concentration impurity region and a high concentration impurity region; and a gate electrode 14 overlapping with the plurality of channel forming regions and some of the plurality of impurity regions with a gate insulating film 13 interposed therebetween.

Otani discloses a display device comprising a thickness of a gate insulating film of a TFT in a driver circuit portion 20a; 20b is thinner than a gate insulating film of a TFT in a pixel portion 20c.

Okabe discloses a display device comprising a first portion of a source wiring 13a overlapped with a gate electrode 12 having a smaller line width than a second portion of said source wiring not overlapped with said gate electrode.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Ikeda's teachings with Matsumoto's device since that would provide a pixel with a larger numerical aperture. It would have been obvious to incorporate the teachings of Otani, since that would execute a high-speed operation and reduce power consumption as taught by Otani. It would have obvious to incorporate Okebe's teachings, since that would reduce the area of the intersecting part as taught by Okebe.

As for claims 5 and 10, the prior art omits that electronic equipment selected from the group consisting of a video camera, a digital camera and other various electronic equipment. However, Examiner takes Official Notice that electronic equipment comprising a display device wherein said electronic equipment selected from the group consisting of a video camera or a digital camera is conventional and well known. Therefore, it would have been obvious to one

skilled in the art at the time the invention was made to have used any of the various electronic equipment since Examiner takes Official Notice that due to their low power consumption, displays have become a necessary and indispensable structural element of an electronic equipment.

As to claims 6, 8 and 24, Ikeda discloses in fig. 3 a plurality of impurity regions 31 comprising a low concentration regions, a high concentration region, and wherein said some of the plurality the low concentration impurity regions and the high concentration impurity region are located between the plurality of the channel forming regions in the semiconductor film or the high concentration impurity region are located between a pair of low impurity regions under the gate electrode (as in claim 24).

As to claims 7, 9, 21-23 and 25, the prior art discloses at least two impurity regions overlapped with the gate electrode and at least one impurity region overlapped with the gate electrode containing an element belonging to group XV in the periodic table (as in claims 22 and 25) but does not specifically disclose having a concentration as recited in the claim. However, it would have been obvious to optimize the device by using a workable range, which involves only a routine skill in the art. Further, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

6. Claims 4 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo US Patent No. 6,140,162 in view of Ikeda (JP 7-326767), Otani (JP 10-56184) and Okabe (JP 63-222443).

Yeo discloses in fig. 3 a display device comprising a pixel portion and a driver portion on a substrate 200, said pixel portion comprising a semiconductor film comprising a channel forming region 41C, a plurality of impurity regions 41L, a source region 41S, and a drain region 41D; and a gate electrode 43G overlapping with the channel forming region, with a gate insulating film 42T interposed therebetween; and a source wiring 45 electrically connected with one of source region and said drain region, wherein a gate insulating film 52 of a TFT in said driver circuit portion and a dielectric 42T of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness, but omits a gate electrode overlapping plurality of channel regions/some of the plurality of impurity regions, a first portion of a source wiring with a smaller line width overlapping a gate electrode and a thicker gate film in a pixel portion than one in a driver circuit portion.

Ikeda discloses (see abstract and figs. 1-5) a display device comprising a semiconductor film having a plurality of channel regions 21 and a plurality of impurity regions 31A-C having the same conductivity type as a source 23 and drain 25 regions (as in claim 23) wherein some of the plurality of impurity regions are located between the plurality of the channel forming regions in the semiconductor film and contain a low concentration impurity region and a high concentration impurity region; and a gate electrode 14 overlapping with the plurality of channel forming regions and some of the plurality of impurity regions with a gate insulating film 13 interposed therebetween.

Otani discloses a thickness of a gate insulating film of a TFT in a driver circuit portion 20a; 20b is thinner than a gate insulating film of a TFT in a pixel portion 20c.

Okabe discloses a display device comprising a first portion of a source wiring 13a overlapped with a gate electrode 12 having a smaller line width than a second portion of said source wiring not overlapped with said gate electrode.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Ikeda's teachings with Matsumoto's device, since that would provide a pixel with a larger numerical aperture. It would have been obvious to incorporate the teachings of Otani, since that would execute a high speed operation and reduce power consumption as taught by Otani. It would have obvious to incorporate Okebe's teachings, since that would reduce the area of the intersecting part as taught by Okebe.

7. Claims 16, 17 and 27-29, as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto US Patent No. 5,323,042 in view of Ikeda (JP 7-326767), Otani (JP 10-56184) and Okabe (JP 63-222443).

Matsumoto discloses in fig. 1 a display device comprising a pixel portion 12 and a driver portion 13 on a substrate 11, said pixel portion comprising a semiconductor film comprising a channel forming region 21a, a plurality of impurity regions 21b, a source region 21c, and a drain region 21c; and a gate electrode 25 overlapping/partially overlapping with the channel forming region and some of the plurality of impurity regions, with a gate insulating film 24 interposed therebetween; and a source wiring 31/32 electrically connected with one of source region and said drain region, wherein a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and

have the same film thickness (as in claim 29), but omits a gate electrode overlapping plurality of channel regions/some of the plurality of impurity regions, a first portion of a source wiring with a smaller line width overlapping a gate electrode and a thicker gate film in a pixel portion than one in a driver circuit portion.

Ikeda discloses (see abstract and figs. 1-5) a display device comprising a semiconductor film having at least two channel forming regions 31A and 31C, at least one first impurity region 21A, at least one second impurity region 21B, a high concentration impurity region 31B, a source region 23, and a drain region 25; wherein one of the two channel forming region is located between the first impurity region and second impurity region; and a gate electrode 14 overlapped with said two channel forming regions and the first impurity region, and a part of the second impurity region with a gate insulating film 13 interposed therebetween.

Otani discloses a display device comprising a thickness of a gate insulating film of a TFT in a driver circuit portion 20a; 20b is thinner than a gate insulating film of a TFT in a pixel portion 20c.

Okabe discloses a display device comprising a first portion of a source wiring 13a overlapped with a gate electrode 12 having a smaller line width than a second portion of said source wiring not overlapped with said gate electrode.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Ikeda's teachings with Matsumoto's device since that would provide a pixel with a larger numerical aperture. It would have been obvious to incorporate the teachings of Otani, since that would execute a high-speed operation and reduce power consumption as

taught by Otani. It would have obvious to incorporate Okebe's teachings, since that would reduce the area of the intersecting part as taught by Okebe.

As for claim 17, the prior art omits that electronic equipment selected from the group consisting of a video camera, a digital camera and other various electronic equipment. However, Examiner takes Official Notice that electronic equipment comprising a display device wherein said electronic equipment selected from the group consisting of a video camera or a digital camera is conventional and well known. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have used any of the various electronic equipment since Examiner takes Official Notice that due to their low power consumption, displays have become a necessary and indispensable structural element of an electronic equipment.

As to claims 27 and 28, the prior art discloses at least two impurity regions overlapped with the gate electrode and at least one impurity region overlapped with the gate electrode containing an element belonging to group XV in the periodic table (as in claim 28) but does not specifically disclose having a concentration as recited in the claim. However, it would have been obvious to optimize the device by using a workable range, which involves only a routine skill in the art. Further, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

8. Claims 18-20 and 30-33 as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto US Patent No. 5,323,042 in view of Ikeda (JP 7-326767), Otani (JP 10-56184) and Okabe (JP 63-222443).

Matsumoto discloses in fig. 1 a display device comprising a pixel portion 12 and a driver portion 13 on a substrate 11, said pixel portion comprising a semiconductor film comprising a channel forming region 21a, a plurality of impurity regions 21b, a source region 21c, and a drain region 21c; and a gate electrode 25 overlapping/partially overlapping with the channel forming region and some of the plurality of impurity regions, with a gate insulating film 24 interposed therebetween, wherein a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness, but omits a gate electrode overlapping plurality of channel regions/some of the plurality of impurity regions, a first portion of a source wiring with a smaller line width overlapping a gate electrode and a thicker gate film in a pixel portion than one in a driver circuit portion.

Ikeda discloses (see abstract and figs. 1-5) a display device comprising a semiconductor film having at least two channel forming regions 21, first low concentration impurity regions 31A, a second low concentration impurity region 31C, a high concentration impurity region 31B, a source region 23, and a drain region 25; wherein the high concentration impurity region is located between the two channel forming regions or between a pair of low concentration impurity regions (as in claim 31); and a gate electrode 14 overlapping with said two channel forming regions, the first low concentration impurity regions, the high concentration impurity

region, and a portion of the second impurity region, with a gate insulating film 13 interposed therebetween.

Otani discloses a display device comprising a thickness of a gate insulating film of a TFT in a driver circuit portion 20a; 20b is thinner than a gate insulating film of a TFT in a pixel portion 20c (as in claim 19).

Okabe discloses a display device comprising a first portion of a source wiring 13a overlapped with a gate electrode 12 having a smaller line width than a second portion of said source wiring not overlapped with said gate electrode.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Ikeda's teachings with Matsumoto's device since that would provide a pixel with a larger numerical aperture. It would have been obvious to incorporate the teachings of Otani, since that would execute a high-speed operation and reduce power consumption as taught by Otani. It would have obvious to incorporate Okebe's teachings, since that would reduce the area of the intersecting part as taught by Okebe.

As for claim 20, the prior art omits that electronic equipment selected from the group consisting of a video camera, a digital camera and other various electronic equipment. However, Examiner takes Official Notice that electronic equipment comprising a display device wherein said electronic equipment selected from the group consisting of a video camera or a digital camera is conventional and well known. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have used any of the various electronic equipment since Examiner takes Official Notice that due to their low power consumption, displays have become a necessary and indispensable structural element of an electronic equipment.

As for claim 30, Ikeda discloses the first low concentration impurity regions 31A, the second low concentration impurity region 31C, and the high concentration impurity region 31B having the same conductivity type as the source 23 and drain 25 regions.

As to claims 32 and 33, the prior art discloses at least two impurity regions overlapped with the gate electrode and at least one impurity region overlapped with the gate electrode containing an element belonging to group XV in the periodic table (as in claim 33) but does not specifically disclose having a concentration as recited in the claim. However, it would have been obvious to optimize the device by using a workable range, which involves only a routine skill in the art. Further, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
July 6, 2004

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